In the Abstract

Replace the Abstract, with the following:

---A cache interface circuit includes a processor interface for receiving memory access requests from a processor, and for transmitting memory data back to the processor in response to processor requests. A main memory interface provides for issuing main memory access requests to a main memory and for receiving main memory data in response. A cache memory interface provides for issuing memory access requests to a cache memory, if operating in a cache mode, and for receiving cache memory data in response. A cache-bypass mode-control signal input provides for the processor to indicate a cache-bypass mode in which memory access requests are serviced from the main memory. A power control output provides for switching off operating power to the cache memory in response to a command received at the cache-bypass mode-control signal input that indicates all memory access requests should be serviced from the main memory.---.

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